

IN THE CLAIMS:

1. (original) A memory controller comprising:

a control unit configured to read data including an associated error correction code from a memory subsystem in response to a memory read request;

a storage unit coupled to said control unit;

an error detection and correction unit coupled to receive said data and configured to determine whether an error exists in said data based upon said associated error correction code;

wherein said control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and

wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from said memory subsystem and to write a corrected version of said data within said memory subsystem.

2. (original) The memory controller as recited in claim 1, wherein said error detection and correction unit is further configured to provide said corrected version of said data in response to said subsequent read of said data.

3. (currently amended) The memory controller as recited in claim 1, wherein said indication includes an address in said memory subsystem of said ~~erroneous~~ data corresponding to said read request.

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